#### UTILITY PATENT

### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Vishwas V. Hardikar Group Art Unit: UNKNOWN

Serial No.: UNKNOWN Examiner: UNKNOWN

Filed: 9/18/2003 Attorney Docket No.: 004.0108

For: METHODS FOR DEPOSITING COPPER ON A NOBLE METAL LAYER

OF A WORK PIECE

# INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P. O. Box 1450 Alexandria, VA. 22313-1450

### Commissioner:

In accordance with 37 C.F.R. § 1.56 and in a manner prescribed by 37 C.F.R. § 1.97 and 1.98, this Information Disclosure Statement IDS is being submitted herewith for consideration by the United States Patent and Trademark Office.

# I. <u>CONTENT</u>

This IDS includes:

- A list of all patents, publications, applications, or other information submitted for consideration by the Office on PTO form SB/08A, which is included herewith;
- A legible copy of: (i) each U.S. patent application publication and U.S. and foreign patent (if required); and (ii) each publication or that portion which caused it to be listed.

I.	CONC	CISE EX	(PLANAT)	ION OF T	HE RELEVA	NCE (check at least one box)	
		explan	ation is no	t required	•	ed in this section II, a concise atents, publications, applications aguage.	
		individ the in	dual design formation,	ated in 1. of all	56(a) most kno	s it is presently understood by the owledgeable about the content of ications, applications or other h language.	
		1 4			f a non-Englisl of an abstract)	h Language document, or portion	
		is listed previous application under	ed on PTC usly cited ations that 35 U.S.C	form SI by or sul has been 120 and	B/08A, which bmitted to the relied on for	olication or other information that are not enclosed herewith were Office in one of the following an earlier effective filing date nitted in the earlier application of 1.98:	
			U.S. Appl	ication Se	erial No.	U.S. Filing Date	
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III.	THIS	IDS IS I	BEING FII	LED UND	DER 37 C.F.R.	1.97(b): (check one box)	
	$\boxtimes$				e filing date of plication under	a national application other than 1.53(d).	
					e date of entry application.	of the national stage as set forth	
		that a this ID charge	first Office OS under 3 deposit a	e Action of 7 C.F.R. ccount	on the merits l	action on the merits. In the event has been mailed, please consider the statement under 1.97(e) or pecified by 37 C.F.R. 1.17(p) if VI.	
		Before the mailing of a first Office Action after the filing of a request for continued examination under 1 114					

IV.	THIS IDS IS BEING FILED UNDER 37 C.F.R. 1.97(c):						
		After the period specified in 37 C.F.R. 1.97(b) and before the mailing date of any of a final action under 1.113, a notice of allowance under 1.311 or an action that otherwise closes prosecution in the application, and accompanied by:					
		a statement specified in 1.97(e) as subsequently provided in this IDS; or					
		the fee set forth in 1.17(p).					
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VI.		nent under 37 C.F.R. 1.97(e) (check only one box) ndersigned hereby states that:					
		Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this IDS.					
		No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this IDS.					
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		A check in the amount of \$ is enclosed for fees due with respect to this IDS.					
		Please charge Deposit Account No in the amount of \$ for the fees due with respect to this IDS. A duplicate copy of this paper is included with this IDS.					

### VIII. CONCLUSION

It is respectfully submitted that the claims presently on file patently distinguish the present invention from each of these references cited in this IDS. The references cited in this IDS are being cited only in the interests of candor and without any admission that they constitute statutory prior art or contain matter which anticipates the invention or which would render the same obvious, either singly or in a combination, to a person of ordinary skill in the art. Furthermore the filing of this IDS should not be construed to be an admission that the information cited in this IDS is, or is considered to be, material to patentability as defined in 1.56(b). In addition, the filing of this IDS should not be construed as a representation that a search has been made.

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Please charge any additional fees or credit any overpayment related to this IDS to Deposit Account No. <u>50-2091</u>.

Respectfully submitted,

Date: September 18, 2003

By: Alorah Henscheid
Deborah K. Henscheid
Reg. No. 35,940

Ingrassia Fisher & Lorenz, P.C.
Customer No. 29906

Enclosures: PTO/SB/08A
References

Foreign Search Report

Fee

Other:

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				Application Numb r	UNKNOWN	
INFO	RMATION D	ISC	LOSURE	Filing Date	09/18/2003	
STAT	<b>TEMENT BY</b>	AP	PLICANT	First Named Inv ntor	Vishwas V. Hardikar	
				Group Art Unit	UNKNOWN	
(use as many sheets as necessary)				Examiner Name	UNKNOWN	
Sheet 1 of 1			1	Attorney Docket Number	004.0108	

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No.1	U.S. Patent Document  Kind Code²  Number (if known)		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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# OTHER ART

### (Including Author, Title, Date, Pertinent Pages, Etc.)

"Electrodeposition of Copper Thin Film on Ruthenium - A Potential Diffusion Barrier for CU Interconnects", Oliver Chyan et al., Journal of The Electrochemical Society, Volume 150, Number 5 (2003)
"Seedless Superfill: Copper Electrodeposition in Trenches with Ruthenium Barriers", D. Josell et al., Electrochemical and Solid State Letters, June 5, 2003
"Liner Materials for Direct Electrodeposition of Cu", M.W.Lane et al., Applied Physics Letter, Volume 83, Number 12, September 22, 2003
"International Technology Roadmap for Semiconductors", 2001